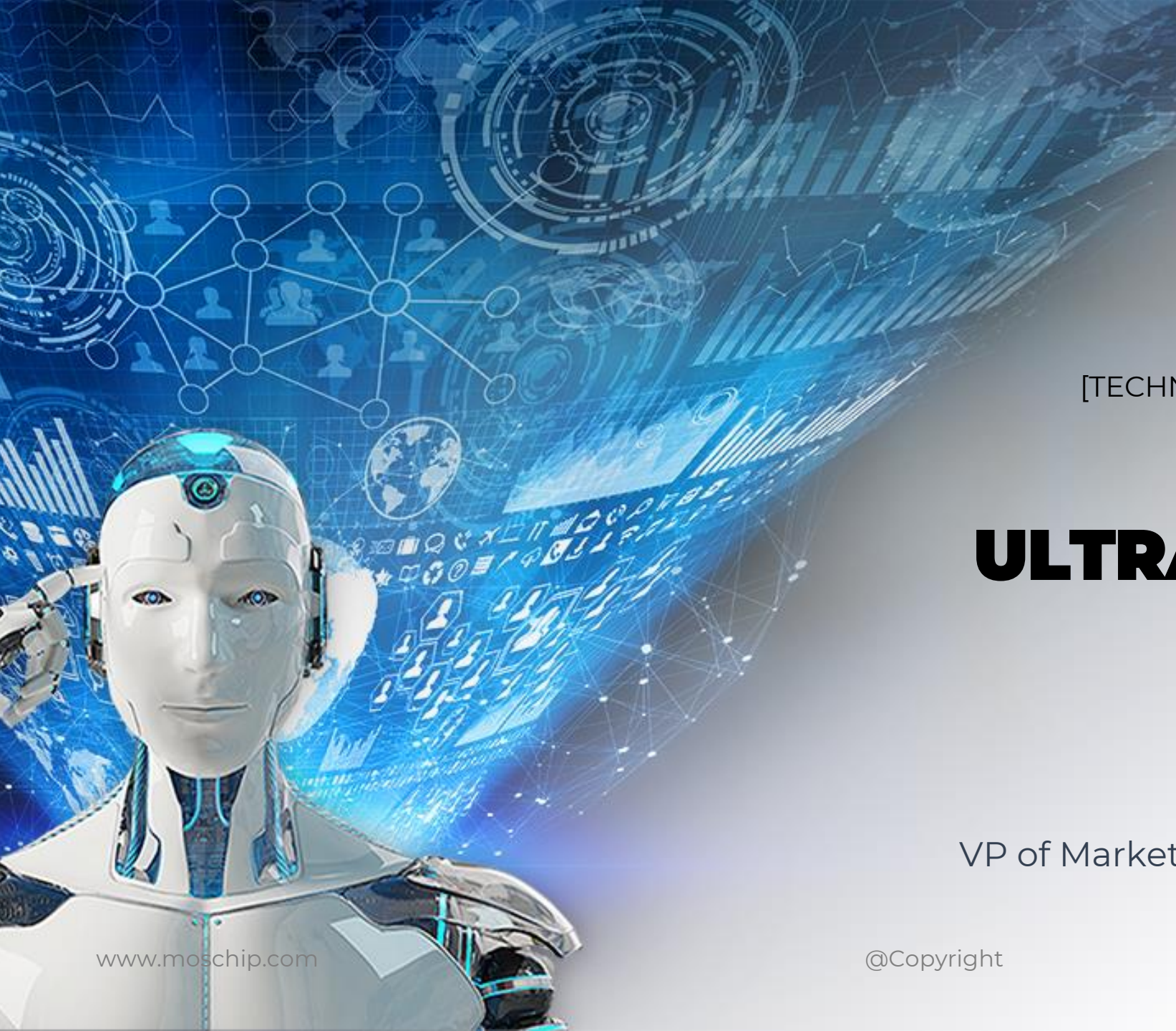


MOSCHIP

IESA AI SUMMIT
Driving Innovation

[TECHNICAL SESSION - AI / ML APPLICATIONS]

ULTRA-LOW POWER EDGE AI ASICS

SWAMY IRRINKI

VP of Marketing and Business Development

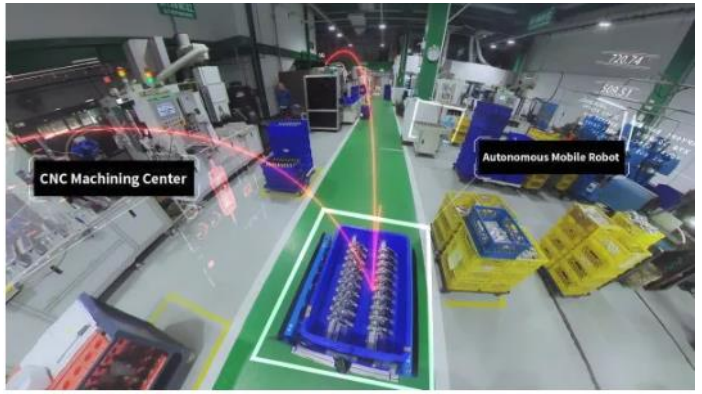
Agenda

- AI Edge Devices End Application Examples
- Edge Accelerator/ASICs for Low Power Edge Devices
- Edge Devices AI Chip Market
- MosChip ASIC Platform for Smart Edge Devices
- Edge Implementation Examples /Demo
- Conclusions
- Q & A

AI Edge Devices End Application Examples

AI Self Checkout

AI Facial Recognition



Autonomous Mobile Robots in Manufacturing

Edge AI Accelerators - Customized for Specific Edge Devices

Pros and cons	Processor		
	CPU	*GPU*	*Edge AI accelerator*
Advantage	• Easily to implement any algorithms	• Can process high throughput video data • High memory bandwidth • High parallel processing ability	• Power and computation efficient • Compact size • Customizable design for the specific application
Disadvantage	• The sequential processing feature does not match the characteristic of CNN, requiring massively parallel computing.	• Requires massive power support • Restricts its application for power-sensitive edge devices • Images in a streaming video and some tracking algorithms are inputted sequentially but not parallel.	• Customizable for the specific targeted application (inflexible for all type computations) • Computational power limited compared to data center CPU and GPU
Application platform	• More suitable for datacenter • Cooperate with AI accelerator	• More suitable for datacenter • Cooperate with AI accelerator	• Customized for specific edge devices • Can cooperate with CPU or GPU

Source: Low-power Ultra-small Edge AI Accelerators for Image Recognition with Convolution Neural Networks: Analysis and Future Directions Weison Lin 1, *, Adewale Adetomi 1 and Tughrul Arslan 1 Institute for Integrated Micro and Nano Systems, University of Edinburgh, Edinburgh EH9 3FF, UK; adewale.adetomi@ed.ac.uk; tughrul.arslan@ed.ac.uk

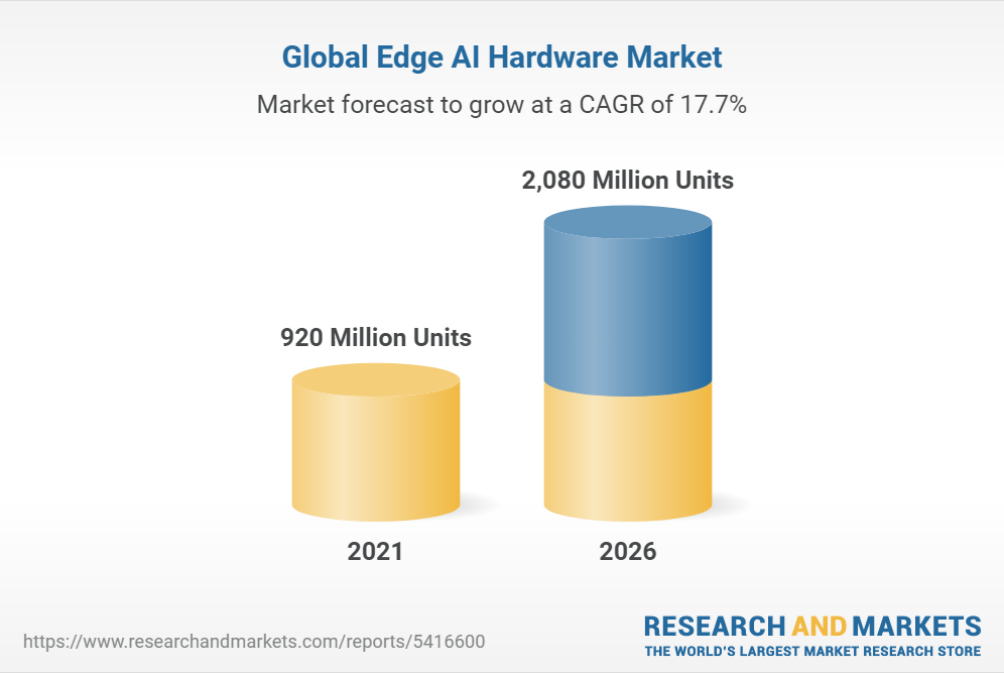
ASIC- High Performance with Low Power Consumption

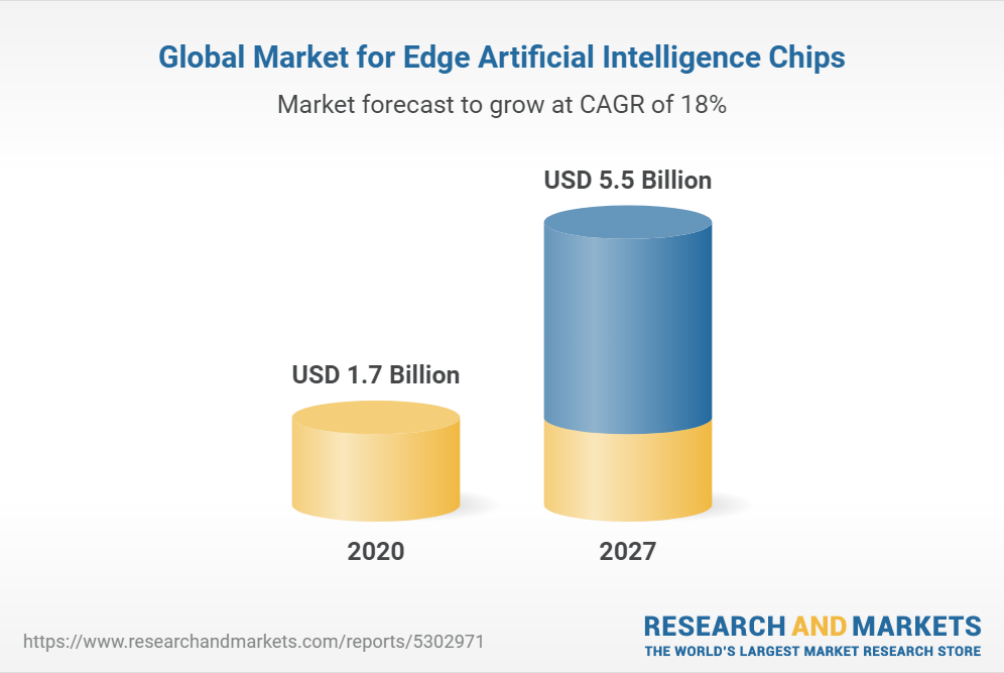
Core Type	Custom ASIC	Typical Power Consumption	Description	Strengths	Constraints
CPU		High	Flexible, general purpose processing units	• Complex instructions and tasks • System management	• Possible memory access bottlenecks • Few cores (4-16)
GPU		High	Parallel cores for high quality graphics rendering	• High performance AI processing • Highly parallel core with 100's or 1,000's of cores	• High power consumption • Large footprint
FPGA		Medium	Configurable logic gates	• Flexible • In-field reprogrammability	• High power consumption • Programming complexity
ASIC		Low	Custom logic designed with libraries	• Fast and low power consumption • Small footprint	• Fixed function • Expensive custom design

Source: https://blog.adlinktech.com/2021/02/19/embedded-hardware-processing-ai-edge-gpu-vpu-fpga-asic

Edge Devices AI Chip Market

ASIC Segment to Record 20.9% CAGR





Type	2027 TAM	CAGR
ASIC	$1B	20.9%
CPU/GPU/FPGA	$4.5B	16.7%

ASICs are Optimized for Ultra-Low Power Sensitive Edge Devices

Cost & Power Sensitive applications

- *Battery Life and Low Cost*
- *Always-On Sensor hub*
- *Addressing privacy concerns through On-device AI*
- *Low-Light Image Processing (RGB-IR) with HDR*

ASIC Development for Ultra-Low Power Edge Devices

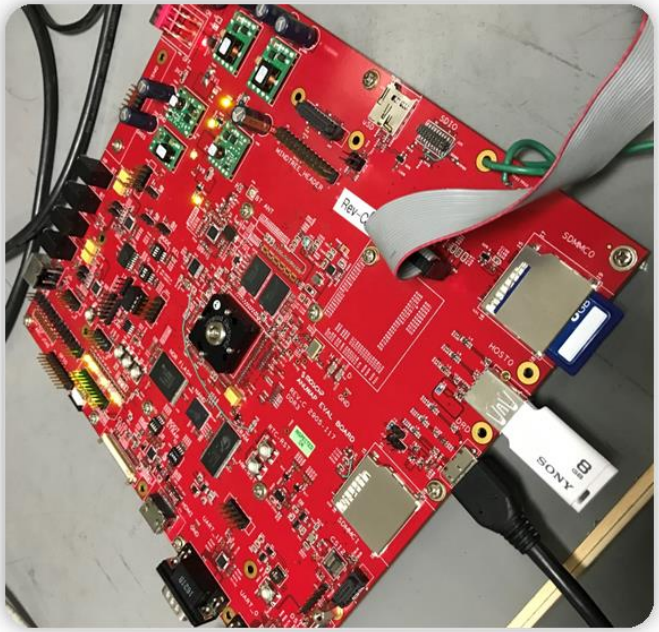
- ASICs enable high-performance processing with low-power consumption and small form factor, a must for edge devices
- ASICs are optimized for a specific application compared to GPU/CPU/FPGAs
- ASICs can deliver AI functionality at a lower unit price point (Requires upfront investment)
- Most of edge device ASICs can be developed in mature process nodes (22nm/28nm and above)

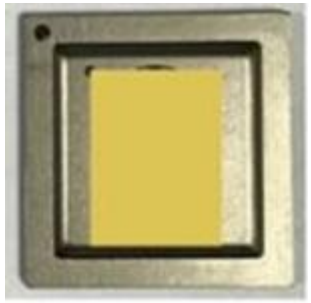
Matrix I – ASIC Platform for Edge Devices (40nm)

- TSMC 40nm
- Flip Chip
- ARM cortex A9 dual core
- Trust Zone Support for ARM
- GPU- Mali 400
- ARC417 video processor
- USB3.0 Host /OTG Controller
- LPDDR2/DDR3 Controller
- SRAM, NAND, NOR controller
- GNSS
- SDIO, SDMMCC
- CLCD Display Controller
- MIPI DSI Controller
- MIPI CSI – II Controller
- Network Interconnect (NIC301)

- 8 Channel DMA
- HDMI 1.4a Rx & HDMI 1.4a Tx
- I2S Controller
- SPI, I2C and UART Controller
- CAN and GPIO Controller
- Keypad/Mouse Controller
- RTC ,WDT, Timer

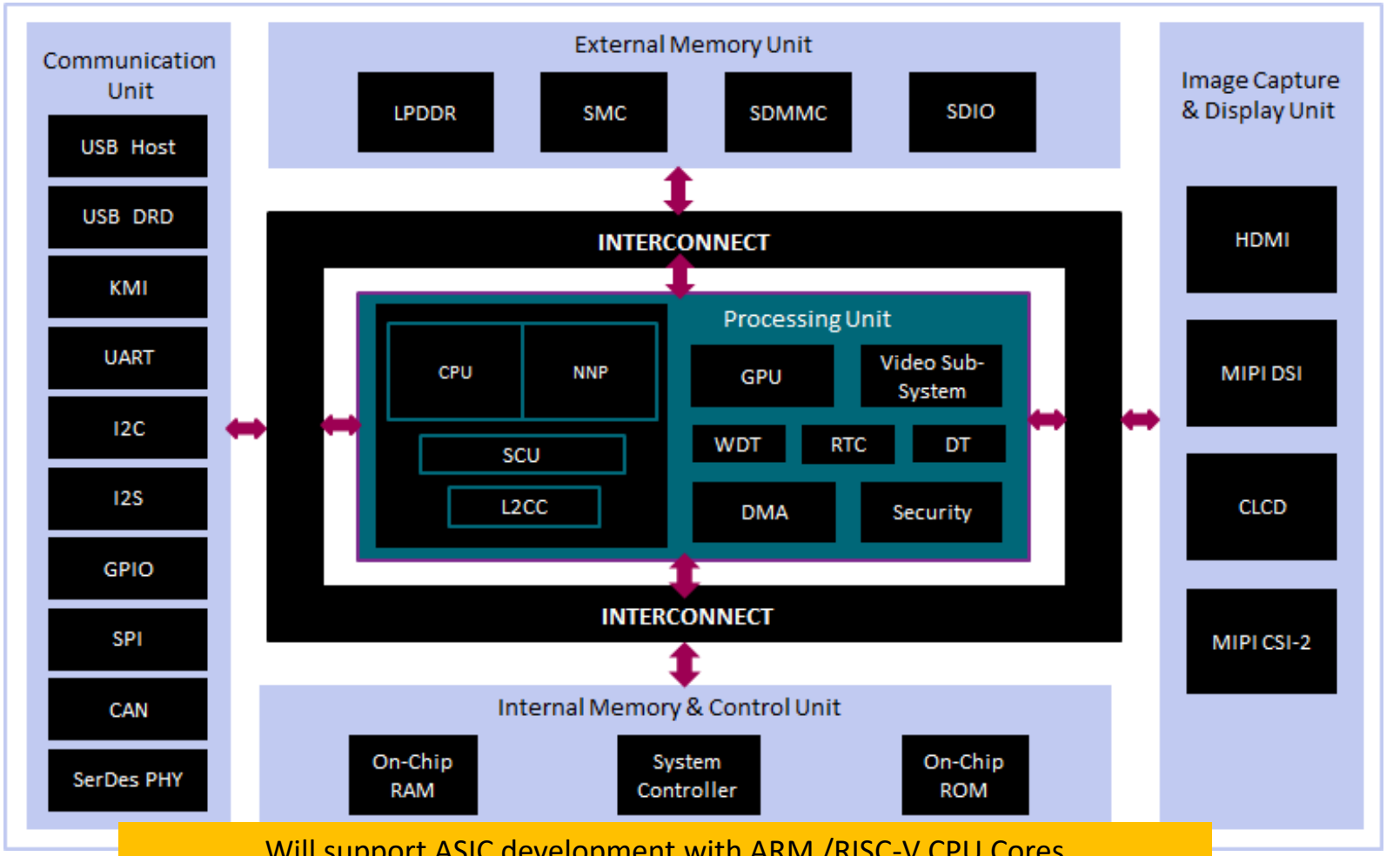
- iBoot Code Development
- UBoot Porting
- Bare-metal drivers for LCD,MIPI CSI, DSI
- Integration of bare metal drivers for IP's
- Linux OS Porting & required drivers
- System boot time optimisation
- Power Management
- Boot Modes (NOR,SD,SPI-Flash,NAND)
- Bare-metal & Linux based test applications





MATRIX II - ASIC PLATFORM FOR ULTRA-LOW POWER SMART EDGE DEVICES (28NM)

BRAINCHIP AKIDA NEURAL NETWORK PROCESSOR (NNP) IP



Will support ASIC development with ARM /RISC-V CPU Cores

MosChip's Mixed Signal and Analog IP for Edge Devices

(Matrix II ASIC Platform)

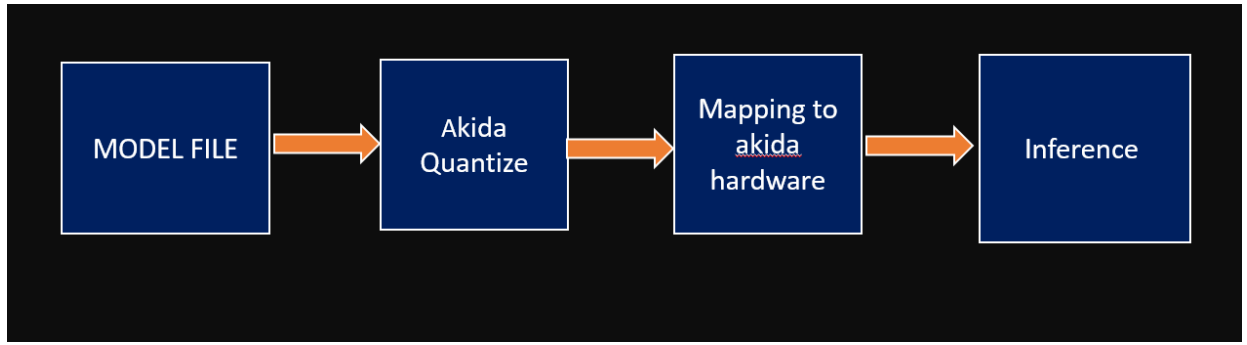
SerDes PHY	Standards	PCS	Data Rate per Lane (Gbps)	Features
PCIe Gen 1	PCIe 1.1	PIPE	2.5	Endpoint or Root Complex PIPE includes skip insertion, deletion PCIe power savings modes
PCIe Gen 2	PCIe 1.1	PIPE	2.5	Endpoint or Root Complex PIPE includes skip insertion, deletion PCIe power savings modes Port bifurcation support
	PCIe 2.0	PIPE	5.0	
XAUI	XAUI, CX4, KX4	Customer	2.4 - 3.2 / 1.2 - 1.6	Generic backplane uses
CEI-6	CEI-6, XAUI, CX4, KX4	Customer	4.8 - 6.4 / 2.4 - 3.2 / 1.2 - 1.6	Generic backplane uses
SATA I/II	SATA I	SATA	1.5	Advanced frequency offset (PPM) compensation for +0 / -0.5% SSC
	SATA II	SATA	3.0	
Switchable	Multiple	Multiple	Multiple	Switchable between 2 or 3 standards Separate interface for each standard
ARM HSSTP	HSSTP 6.0	Aurora Link	6.25 / 12.5	ARM HSSTP PHY along with Link Layer as a single macro
PCIe Gen 3	PCIe 3.0	Partners	8	Backward compatible to Gen2 and Gen1
PCIe Gen 4	PCIe 4.0	Partners	16	Backward compatible to Gen3, Gen2 and Gen1
Chip2Chip		Customer	10	Supports USR (6 dB), VSR(9 dB) and SR(15 dB)
SerialLite	IEEE149.1	PCS	3.125	chip2chip, board2board, shelf2shelf or backplane
Analog IP - ADC/DAC, LVDS I/O, PLLs				

BrainChip's NNP IP Akida is Uniquely Essential
For Ultra-Low Power Edge Devices

- BrainChip's IP fabric can be placed either in a parallelized manner that would be ideal for ultimate performance, or space-optimized in order to reduce silicon utilization and further reduce power consumption.
- Entire neural networks can be placed into the fabric, removing the need to swap weights in and out of DRAM resulting in a reduction of power consumption while increasing throughput.
- Additionally, users can modify clock frequency to optimize performance and power consumption further.

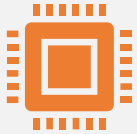
Akida IP Edge Implementation Examples

- Classification
- Detection
- Edge Learning



Demo

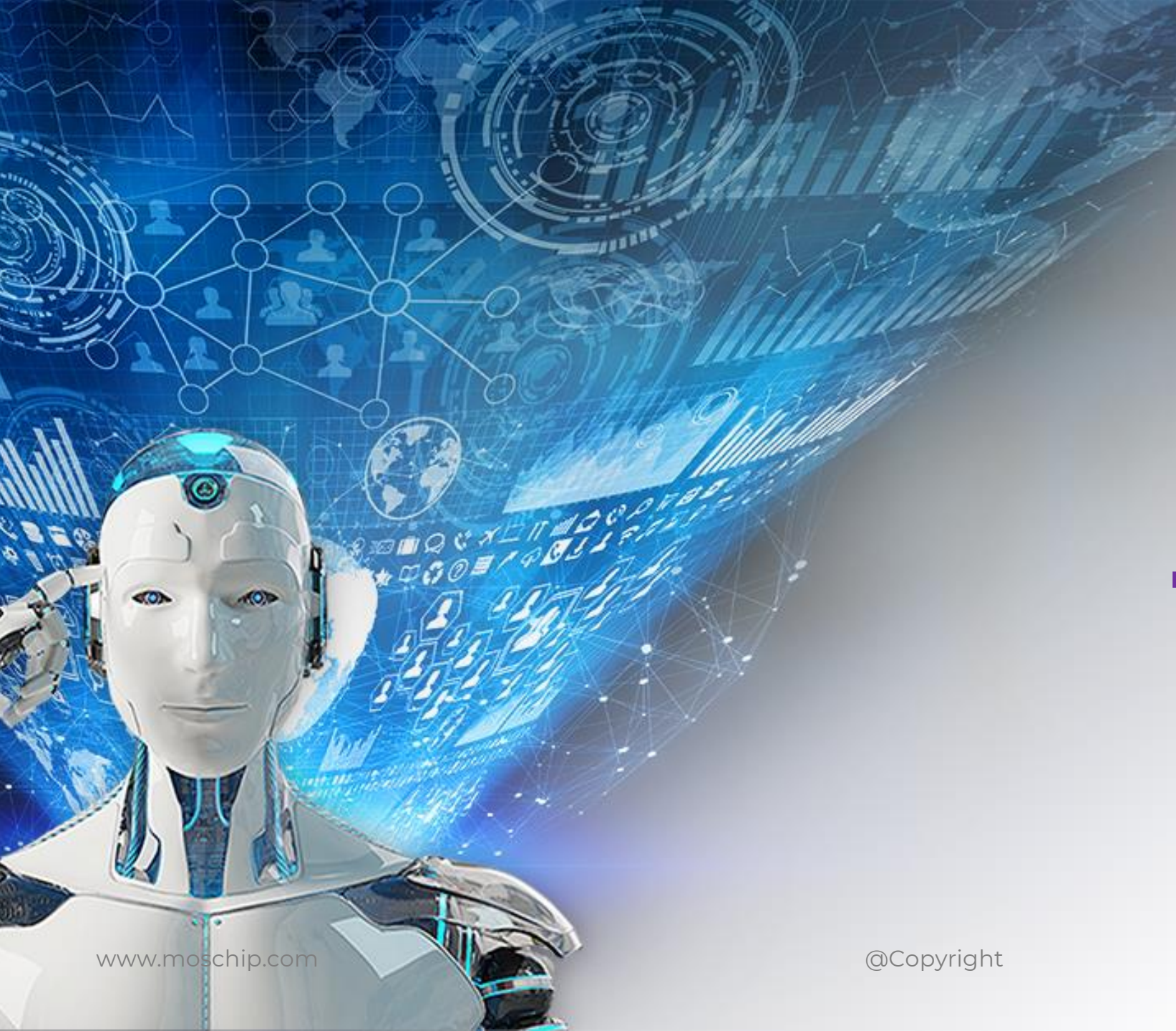
Conclusions



Edge AI Accelerators can be customized for specific edge device/application

ASICs enable high-performance processing with low-power consumption and small form factor

MosChip ASIC Platform with Brainchip's Akida NNP IP will enable customers to develop and bring-up custom SoC solutions for ultra-low power smart edge devices



Thank You